Influence of Dead Time on Voltage Harmonic Spectrum of Grid-Connected PWM-VSC with LCL Filter

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***Abstract*—In recent years, the three-phase pulse width modulation controlled voltage source converter (PWM-VSC) has found its way to wide range of applications, among which renewable energy sources and adjustable speed drives are the most common. In order to achieve low harmonic distortion of current at the point of common coupling (PCC), LCL filters are used for grid connection since they ensure higher damping of current harmonics than L-filters for the same volume. There are many different LCL filter design and optimization methods that are based on the assumption of an ideal converter. Since actual PWM-VSC includes many different sources of nonlinearities, their neglection can potentially lead to selection of inadequate LCL filter in terms of increased grid current harmonic distortion and decreased overall system performance. Research presented in this paper is part of ongoing effort to increase efficiency of adjustable speed drive for crane systems of which the PWM-VSC with LCL filter is a part. This paper focuses on influence of nonlinearities on voltage harmonic spectrum of PWM-VSC. Analysis is carried out by means of nonlinear models and it indicates that the dead time delay has the greatest impact on the system. Validation of simulation results by measurements suggest additional effects should be incorporated into the model. Such a model can then be used for development of more accurate non-iterative LCL filter design and optimization procedures as well as development of operating point optimization algorithms.**

Keywords—dead time, grid-connected pulse width modulation converters, LCL filter, microcontrollers, modeling, power conversion harmonics, simulation

I. INTRODUCTION

The three-phase pulse width modulation controlled voltage source converter (PWM-VSC) is often employed for grid connection of renewable energy sources and adjustable-speed drives using regenerative breaking [1, 2]. The two-level PWM-VSC, realized using IGBT transistors and flyback diodes, can achieve both the rectifier and inverter mode of operation while the AC side voltage can be controlled to adjust the power factor at the point of common coupling (PCC). A filter is needed to obtain these properties and to ensure a low harmonic content of the grid current. LCL filters are often utilized because the same attenuation of grid current harmonics can be achieved with smaller inductors compared to the L filters. The main drawback of the LCL filter is the possibility to excite the current resonance. In order to avoid the resonance problem, passive and active damping methods can be used. Nevertheless, the selection of LCL filter parameters, among other things (selection of control strategy, choice of controller parameters, sampling and carrier frequency) has a major impact on the system performance in dynamic states as well as the overall system stability [3].

The AC voltage harmonic spectrum of an ideal PWM-VSC is solely dependent on the selected modulation technique as well as the synchronization between sampling and PWM algorithm execution [4]. But, in real-time applications, nonlinear voltage errors and distortions are caused by IGBT transistor turn-on and turn-off delays, time delays of IGBT gate driver circuits, the on-state voltage drop of power switches and the dead time delay implemented to avoid the shoot-through of the power switches in an inverter leg [5, 6]. The dead time delay occurs during every PWM period and its influence on VSC's phase leg voltage is proportional to the PWM carrier frequency.

In the past, a number of papers concerning the design of LCL filters for grid-connected PWM-VSC's have been published [7-16]. The most important criterion for the selection of LCL-filter parameters is that the resonant frequency (f_{res}) of the filter should not coincide with the frequencies of the switching harmonics. Recently, several optimization methods for different converter topologies and modulation techniques have been reported in [11-13]. The methods presented in [11, 12] are based on the Virtual Voltage Harmonic Spectrum (VVHS) concept developed in [14]. Based on VVHS and an ideal model of the filter, worst-case grid current harmonic spectrum can be calculated and compared to standards [17, 18]. These optimization methods then employ different criteria to determine the optimal combination of filter parameters from a set of combinations which ensure that grid current harmonic content is within limits defined by standards.

Regardless of the method used, when selecting LCL filter parameters it is common practice to neglect all of the system nonlinearities. This can have significant implications if the optimization of the overall system performance is intended. A system under consideration here is a low-voltage high-power electric drive employed in cranes for the port, harbor, shipyard, container terminal or bulk handling industries intended for continuous operation. Typically, such a drive consists of back-to-back converter, connected to the grid through LCL filter, and an indirect rotor flux oriented squirrel cage induction machine [19]. The research resulting in this paper is a part of

ongoing effort to increase efficiency of LCL filter and converter using the filter parameter optimization procedure and optimization of the operating point. This leads to energy savings while reducing operating costs and emissions considering a long-term exploitation.

In this paper, the influence of different nonlinearities on AC voltage harmonic spectrum of PWM-VSC is analyzed, but the main scope is on the dead-time. The system at hand is presented in Chapter II. In the following Chapter different sources of system nonlinearities are explained. Development of nonlinear model of the observed system is presented in Chapter IV. The obtained simulation results are verified using a laboratory setup described in Chapter V. The comments on future work are drawn in Conclusions.

II. SYSTEM DESCRIPTION

A. System Configuration

The system investigated in this paper is shown in Fig. 1 and its parameters are listed in Tab. 1. As can be seen, a three-phase PWM-VSC is connected to the grid through LCL filter. The converter model includes nonlinearities that are going to be explained later in this Chapter. The grid is modelled with equivalent impedance and an ideal three-phase sinusoidal voltage source (v_{ag}, v_{bg}, v_{cg}) with fundamental frequency (f_n). PWM-VSC is assembled from six semiconductor switches with each consisting of an IGBT transistor and a diode. The LCL filter inductors and capacitor are represented with combined impedances. Parameters L_{fg} and R_{fg} represent the grid-side inductor while L_{fc} and R_{fc} represent the converter-side inductor. Parameters C_{fd} and R_{fd} represent the filter capacitor.

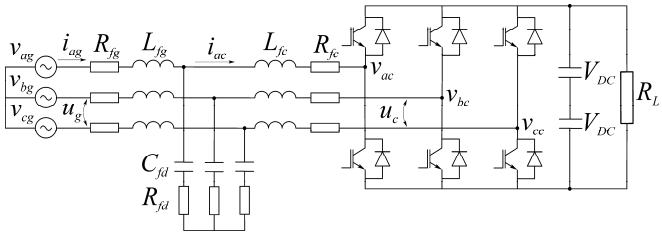

Fig. 1. Three-phase PWM-VSC connected to the grid by LCL filter.

TABLE I. THE PARAMETERS OF SYSTEM SHOWN IN FIG. 1

Symbol	Quantity	Value
U_n	Rated grid voltage (line-to-line, rms)	400 V
f_n	Rated grid frequency	50 Hz
I_n	Rated filter current (rms)	60 A
L_{fg}	Inductance of grid-side filter inductors	0.6 mH
R_{fg}	Resistance of grid-side filter inductors	8 mΩ
L_{fc}	Inductance of converter-side inductors	1.8 mH
R_{fc}	Resistance of converter-side inductors	16 mΩ
C_{fd}	Filter capacitance	60 μF
R_{fd}	Capacitor equivalent series resistance	10 mΩ
C_{DC}	Equivalent DC link capacitance	2200 μF
f_c	Carrier frequency	3 kHz
$2V_{DC}$	DC link voltage	610 V

B. Sources of Converter Nonlinearities

Correlation between the fundamental harmonic of the converter's AC voltage and its referent value represents basic steady-state characteristic of PWM-VSC. Converter non-linearity is observed in such a manner that the aforementioned quantities are not linearly proportional. Main sources of converter nonlinearities are the dead time delay and the on-state voltage drop of power switches. Other sources of nonlinearities may include turn-on and turn-off delays of power switches, the control algorithm computational delay and the propagational delay of electronic circuits.

Since the commutations of real power switches require a finite amount of time, it is necessary to implement a delay between IGBT transistors gate signals in order to avoid the simultaneous conduction of both switches in a converter phase leg. This delay is commonly referred to as the dead time delay. Omission of the dead time delay from the modulator algorithm would lead to converter failure caused by uncontrolled current circulation through the switches due to DC bus short circuit. In modern VSCs dead time delay is ranging between 2 and 8 μs [20]. Effect of dead time delay on converter's AC voltage can be analyzed considering a single phase leg of a three-phase VSC shown in Fig. 2. Corresponding pulse patterns for transistors T_1 and T_2 as well as the phase leg voltage are shown in Fig. 3.

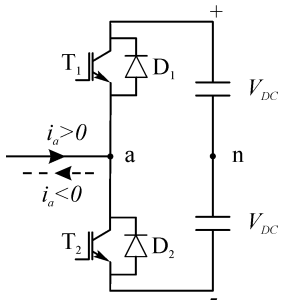

Fig. 2. Single phase leg of three-phase PWM-VSC.

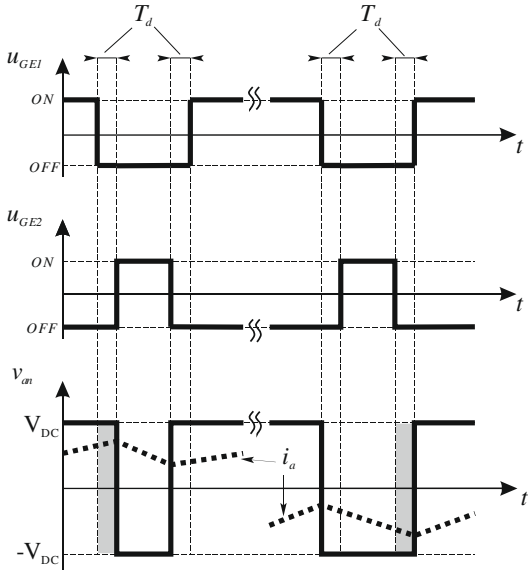

Fig. 3. Practical pulse patterns corresponding to transistors T_1 and T_2 in Fig. 1 illustrating the effect of dead time delay.

It is clear that there are four possible commutation sequences but the effect of dead time delay will depend on the direction of current through the phase leg under observation. First, let us consider that the current is positive ($i_a > 0$ in Fig. 2) and that transistor T_1 transitions from ON to OFF state while transistor T_2 transitions from OFF to ON state after a delay equal to the dead time (T_d). During this delay both transistors are in OFF state and diode D_1 conducts the current. At the same time, the phase leg voltage v_{an} is equal to V_{DC}. If the dead time was equal to zero, i.e. $T_d = 0$, then the phase leg voltage v_{an} would be equal to $-V_{DC}$. The shaded area in Fig. 3 represents the loss of phase leg voltage during this commutation sequence. For the same current direction let us consider second commutation sequence when transistor T_2 transitions from ON to OFF state while transistor T_1 transitions from OFF to ON state after T_d. During this time period D_1 conducts and v_{an} is equal to V_{DC} as it would be the case if the dead time was equal to zero. If we now consider that the current is negative ($i_a < 0$), the loss of phase leg voltage will occur during the commutation sequence when T_2 transitions from ON to OFF and T_1 transitions from OFF to ON after T_d. The phase leg voltage loss can be represented with a series of error pulses that will subsequently lead to occurrence of additional components in the AC voltage harmonic spectrum.

The on-state voltage drop of power switches is usually in the range from 0.5 to 2 V, but it can have a significant impact on converter's characteristics if the converter is operating with a low modulation index. However, the operation of PWM-VSC connected to the grid through LCL filter is characterized by relatively high modulation index since the lower values would correspond to higher currents at PCC. Consequently, the on-state voltage drop of power switches has a constrained influence on converter's AC voltage spectrum.

III. LCL Filter Design Methods

LCL filter design methods are used to select filter parameters according to the chosen criteria which are often defined on the assumption of an ideal system. Since this is not the case with an actual system, implementation of different criteria can lead to selection of filter parameters that could be inadequate due to increased current harmonic distortion at PCC.

A. Filter Parameters Constraints

The procedures used to determine LCL filter parameters include various constraints concerning the filter resonant frequency, the converter AC current ripple, the voltage drop across the filter inductors and the reactive power of filter capacitors. Although they are widely used, these quantities are not defined by standards. Abovementioned constraints are used to define maximum and/or minimum allowed values of filter parameters.

In order to ensure stable operation of the overall system, the following condition should be met

$$(10 \cdot f_n \text{ or } 0.25 \cdot f_c) < f_{res} < (0.5 \cdot f_c) \qquad (1)$$

The combined filter inductance is determined according to voltage drop at rated load and is usually chosen between 5 and 20% of the grid voltage in order not to limit the converter's operation in the PWM linear region [7].

The maximum value of the converter's AC current ripple ($\Delta I_{c,max}$) is used to determine the minimum inductance value of the grid side inductor in accordance with [9, 11]

$$L_{fc,\min} = V_{DC} / (k \cdot f_c \cdot \Delta I_{c,\max}) \qquad (2)$$

where coefficient k depends on the selected PWM technique.

The maximum capacitance of the filter capacitors is selected in such a manner as to limit the reactive power at fundamental frequency and is given by [15, 16]

$$C_{fd,\max} = \lambda \cdot P_n / (6\pi \cdot f_n \cdot U_n^2) \qquad (3)$$

where P_n is the converter rated power and coefficient λ depends on the maximum reactive power. The value of coefficient λ is usually varied between 0.05 and 0.1.

B. Filter Parameters Optimization Methods

Most filter design methods use a number of different constraints, some of them given in previous section, as a starting point of the design process. However, filter optimization methods require selection of criteria which are used to obtain the optimal combination of filter parameters from a set of allowed parameter combinations. These methods often use analytical expressions to compute AC voltage harmonic spectrum of an ideal converter in order to obtain the current harmonic spectrum at PCC. Whether this is done for a single operating point or over entire range of operating points, like in VVHS concept, system nonlinearities are always neglected [11-13]. Thus, inclusion of nonlinearities is expected to result with less erroneous filter design method.

IV. Simulation Modeling and Analysis

A. Nonlinear Model

In order to investigate the influence of different sources of nonlinearities on PWM-VSC's AC voltage harmonic spectrum, the nonlinear model of the system shown in Fig. 1 is developed using simulation program PLECS [21]. Parameters of the nonlinear model correspond to the ones of the experimental setup and are listed in Table 1. Sources of system nonlinearities described in Section II are modelled according to [20, 22]. For the sake of simplification, control structure is omitted from simulation model and the space vector pulse width modulation (SVPWM) is used to generate IGBT control signals based on the referent signal given by modulation index (M) and fundamental reference angle (θ_1). The inherent characteristic of the commonly used voltage oriented control (VOC) structure is compensation of the voltage drop caused by dead time at fundamental frequency [23]. Thus, this is also implemented in the model [4].

Simulation model validation is performed using analytical expressions given in [4] and also by an independently developed algorithm to synthesize converter's AC voltage waveform implemented in MATLAB. If an ideal system is assumed, development of analytical expressions for a given modulation technique and synchronization method between

sampling and PWM algorithm execution requires reformulation of mathematics that define the PWM waveform to be able to use the double Fourier series method [24]. For a given PWM algorithm, every synchronization method will ultimately lead to different harmonic spectrum of the converter's phase leg voltage. Although, this approach provides accurate results, it is obtained at the expense of numerical efficiency. In other words, calculation of double Fourier series coefficients is time consuming in order to achieve satisfactory accuracy. In practice, assumption of an ideal converter is not applicable and sources of nonlinearity should be taken into account when determining harmonic spectrum of the converter's phase leg voltage. To avoid these drawbacks, simulation model in MATLAB is used. It is important to note that this model, as well as the model in PLECS, also provides accurate results while maintaining a higher degree of numerical efficiency than the strictly analytical approach. In addition, usage of MATLAB or PLECS allows for a simpler implementation of different sources of nonlinearities in simulation models. These algorithms are developed with intention to replicate operation of the microcontroller's PWM module used in laboratory setup [25].

The two commonly used methods for synchronization between sampling and PWM algorithm execution are implemented in the models [24-26]. These synchronization methods involve different updating and sampling concepts. In this paper, only PWM with a triangular (double-edge) waveform carrier signal is considered.

B. Simulation Results

Influence of sources of nonlinearities has been analyzed for various operating points (different loads and power factors at PCC). Furthermore, analysis has been carried out for different carrier frequencies as well as for two synchronization methods: (1) double-edge single-update symmetrical regular sampled PWM and, (2) double-edge double-update asymmetrical regular sampled PWM. In order to illustrate the effect of nonlinearities, only results obtained for rectifier mode of operation at unity power factor and rated current are presented because the similar conclusions can be made for all operating points. Double edge single-update symmetrical regular sampled SVPWM is used for results presented in this section since it generates additional harmonic components compared to asymmetrical regular sampled SVPWM and is therefore more suitable for analysis. Furthermore, an ideal grid is assumed as well as constant DC link voltage.

Fig. 4a shows the averaged line-to-line voltage harmonic spectrums of VSC in case of an ideal converter (1) and, when the dead time delay (2) or the power switches voltage drop (3) is implemented in the model. Carrier frequency is 3 kHz, while the dead time and the power switches voltage drop are selected according to laboratory setup data [20, 22]. In case of an ideal converter simulation results are consistent with the modulation theory of three-phase VSC. In other words, all carrier and triplen sideband harmonics are cancelled out in the line-to-line voltage spectrum since they are equal for all phase legs [4].

As can be seen from Fig. 4a, due to implementation of nonlinearities, additional components are generated throughout the voltage harmonic spectrum. For both cases under consideration, most important differences are observed in the baseband region at frequencies given by $(6n \pm 1)\cdot f_n$, where n = 1, 2, 3, … Moreover, implementation of the dead time subsequently leads to greater difference in harmonic magnitudes compared to the ideal converter than the implementation of power switches voltage drop. Comparing the influence of the abovementioned sources of nonlinearity, it can be stated that the power switches voltage drop can be omitted from simulation model.

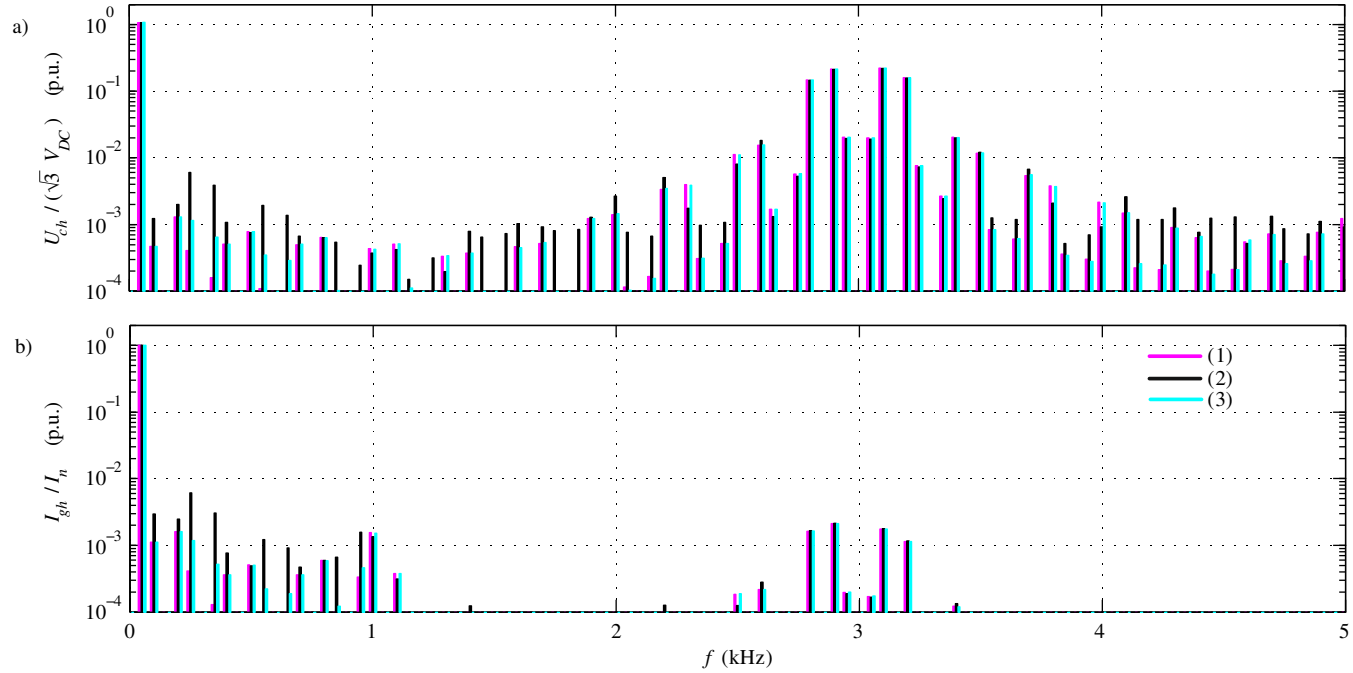

Fig. 4. PWM-VSC's voltage (a) and grid current (b) harmonic spectrums: (1) ideal converter, (2) included dead time, (3) included power switches voltage drop.

Fig. 4b shows the averaged grid current harmonic spectrums corresponding to Fig. 4a. Higher order current harmonics are filtered out by LCL filter while the baseband and the first sideband harmonics remain present in the spectrum. As expected, most significant changes of harmonic magnitudes appear on frequencies given by $(6n \pm 1)\cdot f_n$. Harmonics located around 1 kHz are affected by the LCL filter resonant frequency (968 Hz).

Although, grid current harmonic magnitudes may appear relatively low compared to the nominal current, it should be pointed out that the grid current harmonic limits defined by standards are very stringent [17, 18]. Because of this, Fig. 5 presents averaged magnitudes of certain grid current baseband harmonics, related to the values allowed by standards, with and without implementation of the dead time for different carrier frequencies. In Fig. 5, h represents harmonic order. Increase of carrier frequency results in higher magnitudes of harmonics when the dead time is implemented. This is expected since the ratio of dead time to PWM period increases.

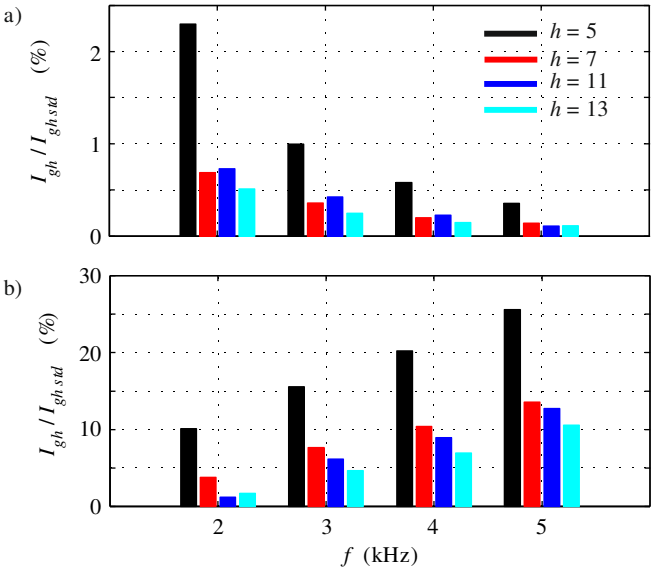

Fig. 5. Selected grid current harmonics magnitude: a) ideal converter, b) included dead time.

V. Experimental Setup and Measurements

A. Laboratory Setup

Parts of the electric regenerative drive employed in crane systems are used to construct laboratory setup which consists of 50 kW adjustable resistive load connected to DC link bus of the back-to-back converter while the motor side is disconnected. On the other side, the converter is connected to the grid through LCL filter. Voltage oriented control of the grid side PWM-VSC is implemented in Texas Instruments' TMS320F28335 microcontroller. Differences between IGBT turn-on and turn-off delays are compensated by the IGBT gate driver circuits. Thus, these delays have no significant impact on the converter's AC voltage harmonic spectrum and also have no influence on other sources of nonlinearities. The dead time delay can be arbitrarily chosen and 4 μs is selected for experimental analysis according to IGBT manufacturer's recommendations.

The voltage differential and current probes are used to measure grid and converter voltages and currents. Data acquisition is performed using commercially available system of 8 simultaneous sample and hold 12-bit A/D converters. The sample rate of 20 MS/s per channel is used to analyze the measured data. Such data acquisition system is capable of performing continuous streaming measurements and allows for on-line and off-line signal processing. The main advantage of the off-line signal processing is that it allows application of various FFT algorithms on recorded data. Validation of measurement results is carried out by means of Hewlett Packard's digital signal analyzer HP35665A.

B. Experimental Results

Experimental analysis has been carried out for various operating points, considering different loads and power factors at PCC, of PWM-VSC in rectifier mode of operation. Double edge single-update symmetrical regular sampled SVPWM has been used in laboratory setup for the sake of comparison with simulation results. Fig. 6 shows averaged harmonic spectrums of PWM-VSC's line-to-line voltages and grid currents at unity power factor. The grid current fundamental harmonic is 50 Arms while the converter's DC bus voltage is 610 V.

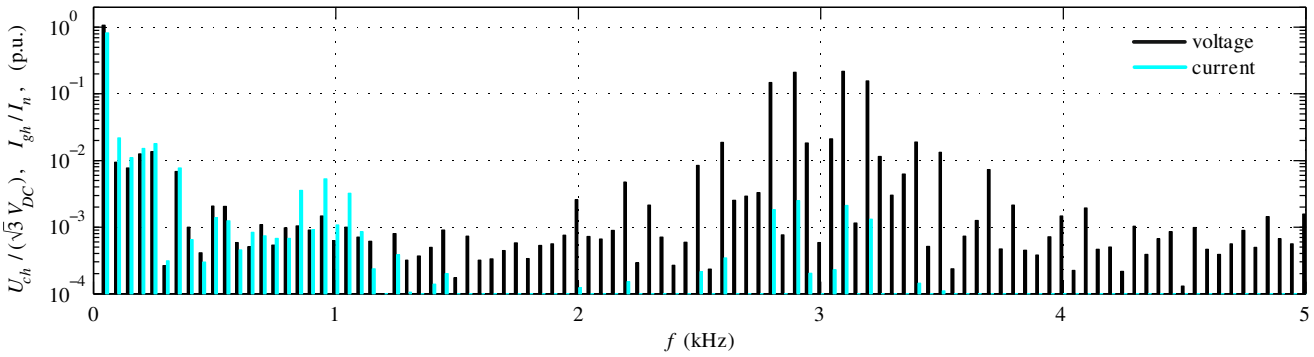

Fig. 6. Measured harmonic spectrums of PWM-VSCs' line-to-line voltage and grid current for unity power factor at PCC.

It is important to note that, by means of laboratory setup, only combined effect of all nonlinearities can be analyzed. As can be seen from Figs. 4 and 6, by comparing experimental and simulation results, it is evident that analytical expressions commonly used in LCL filter design methods do not provide accurate description of the system at hand [9, 16]. Also, discrepancies in the baseband region between simulation and experimental results suggest additional effects should be taken into account by model. First of all, this is related to higher frequency harmonics of the grid voltage and oscillations in the DC bus voltage that are observed in laboratory setup. Moreover, influence of the control system should also be considered.

VI. CONCLUSIONS

In this paper, influence of different nonlinearities on AC voltage harmonic spectrum of grid-connected PWM-VSC is analyzed. The analysis of simulation results indicates that the dead time delay has the most significant individual influence on the grid current harmonic content among considered nonlinearities. Although, analysis by means of nonlinear model suggests that influence of other nonlinearities is less pronounced, comparison of experimental and simulation results indicate that further improvements of the model can be made. Furthermore, experimental results clearly show large discrepancies when compared to ideal representation of the system by analytical expressions. In particular, this is more evident in the baseband region of the AC voltage and current harmonic spectrums. The future work will involve inclusion of DC bus and grid voltage harmonics as well as control structure into the model. Although, these effects were not considered during model development in this paper, their occurrence in an actual system is not unexpected. Such a model could be used to develop a more accurate non-iterative LCL filter design and optimization procedure.

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